TL06xx Low-Power JFET-Input Operational Amplifiers

1 Features

- Very low power consumption
- Typical supply current: 200 µA (per amplifier)
- Wide common-mode and differential voltage ranges
- Low input bias and offset currents
- Common-mode input voltage range includes V_{CC+}
- Output short-circuit protection
- High input impedance: JFET-input stage
- Internal frequency compensation
- Latch-up-free operation
- High slew rate: 3.5 V/µs typical
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Tablets
- White goods
- Personal electronics
- Computers

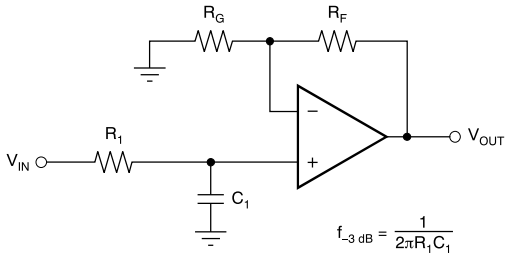
3 Description

The TL06x (TL061, TL062, and TL064) family of industry-standard operational amplifiers (op amps) mirror the TL07x and TL08x family of op amps with lower power consumption. These devices provide outstanding value for cost-sensitive applications, featuring high input impedance, wide bandwidth, high slew rate, and low input offset and input bias currents. High ESD (1.5 kV, HBM), integrated EMI and RF filters, and wide temperature operation enable the TL06x devices to be used in rugged and environmentally-demanding applications.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)	PACKAGE SIZE(2)
TL061x	Single	D (SOIC, 8)	4.90 mm × 6.00 mm
		P (PDIP, 8)	9.59 mm × 7.94 mm
		PS (SO, 8)	6.20 mm × 7.80 mm
TL062x	Dual	D (SOIC, 8)	4.90 mm × 6.00 mm
		P (PDIP, 8)	9.59 mm × 7.94 mm
		PS (SO, 8)	6.20 mm × 7.80 mm
		JG (CDIP, 8)	9.58 mm × 7.62 mm
		PW (TSSOP, 8)	3.00 mm × 6.40 mm
		FK (LCCC, 20)	8.89 mm × 8.80 mm
TL064x	Quad	D (SOIC, 14)	8.65 mm × 6.00 mm
		J (CDIP, 14)	19.4 mm × 7.90 mm
		N (PDIP, 14)	19.31 mm × 7.94 mm
		NS (SO, 14)	10.20 mm × 7.80 mm
		PW (TSSOP, 14)	5.00 mm × 6.40 mm
		W (CFP, 14)	21.78 mm × 9.21 mm
		FK (LCCC, 20)	8.89 mm × 8.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

Single-Pole, Low-Pass Filter

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (June 2023) to Revision N (August 2023)	Page
• Added typical specification for Unity-Gain Bandwidth in *Electrical Characteristics for TL06xM*	10
• Changed Equivalent Input Noise Voltage vs Frequency curve in *Typical Characteristics* section	11

Changes from Revision L (May 2015) to Revision M (June 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated *Device Information* with package size and channel count, and reordered packages based on channel count	1
• Updated TL061 pinout diagram in *Pin Configuration and Functions*	4
• Changed Charged Device Model (CDM) ESD from 2 kV to 1.5 kV in *ESD Ratings*	6
• Added table note for input bias current and input offset current on *Electrical Characteristics for TL06xC and TL06xxC*	8
• Added table note for input bias current and input offset current on *Electrical Characteristics for TL06xxC and TL06xI*	9
• Changed name of *Electrical Characteristics for TL06xM and TL064M* to *Electrical Characteristics for TL06xM*	10
• Added table note for input bias current and input offset current on *Electrical Characteristics for TL06xM*	10
• Changed typical input voltage noise density at 1 kHz from 42 nV/$\sqrt{\text{Hz}}$ to 30 nV/$\sqrt{\text{Hz}}$	10
• Updated description in *Overview*	15
• Updated image in *Functional Block Diagram*	15

Changes from Revision K (January 2014) to Revision L (May 2015)	Page
• Added *Applications*	1
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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Changes from Revision J (September 2004) to Revision K (January 2014) **Page**

- Updated document to new TI data sheet format - no specification changes.....1
- Deleted *Ordering Information* table.....1
- Updated *Features* with Military Disclaimer.....1

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5 Pin Configuration and Functions

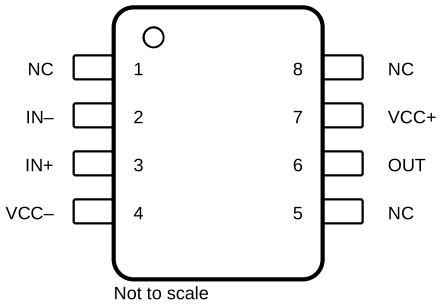

Figure 5-1. TL061x D, P, and PS Package, 8-Pin SOIC, PDIP, and SO (Top View)

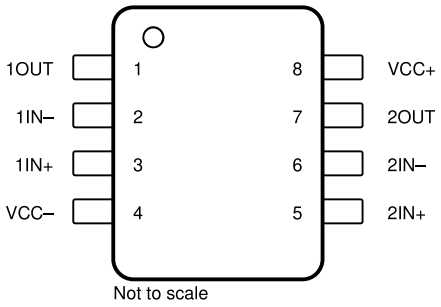

Figure 5-2. TL062x D, JG, P, PS, and PW Package, 8-Pin SOIC, CDIP, PDIP, SO, and TSSOP (Top View)

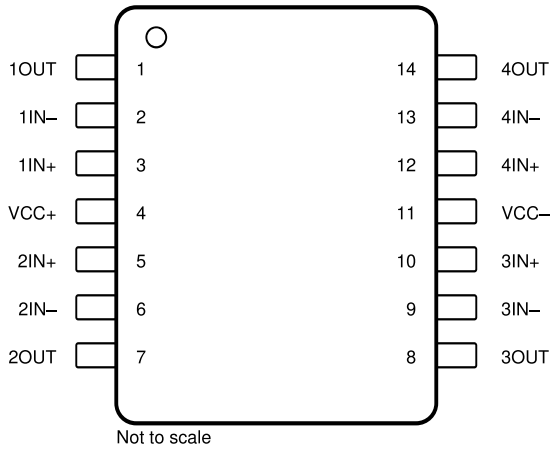

Figure 5-3. TL064x D, J, N, NS, PW, and W Package, 14-Pin SOIC, CDIP, PDIP, SO, TSSOP and CFP (Top View)

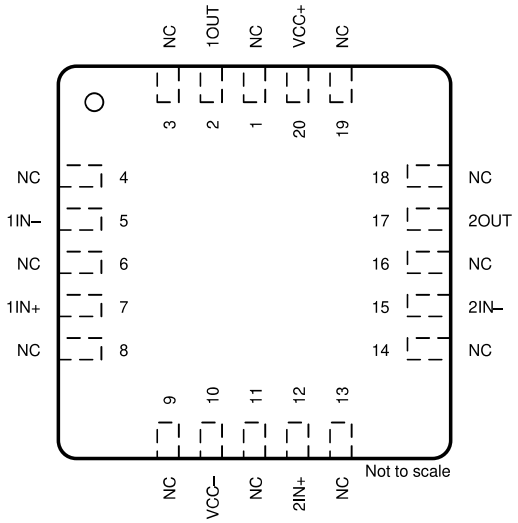

Figure 5-4. TL062 FK Package, 20-Pin LCCC (Top View)

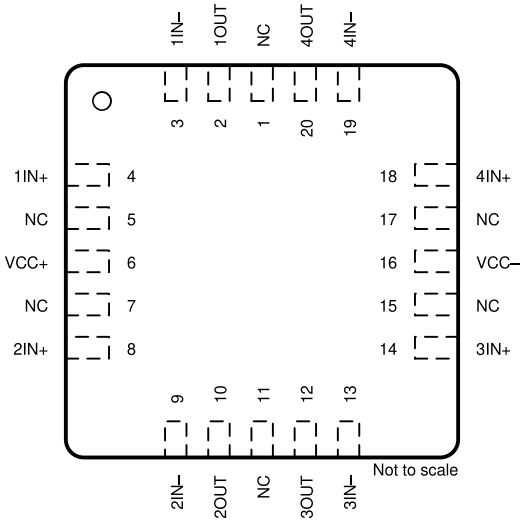

Figure 5-5. TL064 FK Package, 20-Pin LCCC (Top View)

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Table 5-1. Pin Functions

PIN						TYPE[1]	DESCRIPTION
NAME	TL061	TL062		TL064			
	D, P, PS	D, JG, P, PS, PW	FK	D, J, N, NS, PW, W	FK		
1IN–	—	2	5	2	3	I	Negative input
1IN+	—	3	7	3	4	I	Positive input
1OUT	—	1	2	1	2	O	Output
2IN–	—	6	15	6	9	I	Negative input
2IN+	—	5	12	5	8	I	Positive input
2OUT	—	7	17	7	10	O	Output
3IN–	—	—	—	9	13	I	Negative input
3IN+	—	—	—	10	14	I	Positive input
3OUT	—	—	—	8	12	O	Output
4IN–	—	—	—	13	19	I	Negative input
4IN+	—	—	—	12	18	I	Positive input
4OUT	—	—	—	14	20	O	Output
IN–	2	—	—	—	—	I	Negative input
IN+	3	—	—	—	—	I	Positive input
NC	8	—	1	—	1	—	Do not connect
			3				
			4		5		
			6				
			8		7		
			9				
			11		11		
			13				
			14		15		
			16				
			18		17		
			19				
OFFSET N1	1	—	—	—	—	—	Input offset adjustment
OFFSET N2	5	—	—	—	—	—	Input offset adjustment
OUT	6	—	—	—	—	O	Output
$V_{CC–}$	4	4	10	11	16	—	Power supply
V_{CC+}	7	8	20	4	6	—	Power supply

(1) I = input, O = output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)			18	V
V_{CC-}				–18	
V_{ID}	Differential input voltage(3)			±30	V
V_I	Input voltage(2) (4)			±15	V
	Duration of output short circuit(5)		Unlimited		
T_J	Operating virtual junction temperature			150	°C
	Case temperature for 60 seconds	FK package		260	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J, JG, U, or W package		300	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D, N, NS, P, PS, or PW package		260	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+, with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or to either supply. Temperature or supply voltages must be limited so that the dissipation rating is not exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
V_{CC-}	Supply voltage		–5	–15	V
V_{CM}	Common-mode voltage		V_{CC-} + 4	V_{CC+} – 4	V
T_A	Ambient temperature	TL06xM	–55	125	°C
		TL06xQ	–40	125	
		TL06xI	–40	85	
		TL06xC	0	70	

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6.4 Thermal Information (TL061)

THERMAL METRIC[1]		TL061		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2] [3]	97	85	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[4] [5]	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.
(4) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JC}$, and T_C. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_C) / R_{\theta JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(5) The package thermal impedance is calculated in accordance with MIL-STD-883.

6.5 Thermal Information (TL062)

THERMAL METRIC[1]		TL062						UNIT
		D (SOIC)	P (PDIP)	PS (SO)	PW (TSSOP)	FK (LCCC)	JG (CDIP)	
		8 PINS	8 PINS	8 PINS	8 PINS	20 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2] [3]	97	85	95	149	—	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[4] [5]	—	—	—	—	5.61	14.5	°C/W

6.6 Thermal Information (TL064)

THERMAL METRIC[1]		TL064								UNIT
		D (SOIC)	N (PDIP)	NS (SO)	PS (SO)	PW (TSSOP)	FK (LCCC)	J (CDIP)	W (CFP)	
		14 PINS	14 PINS	14 PINS	8 PINS	14 PINS	20 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2] [3]	86	80	76	95	113	—	—	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[2] [3]	—	—	—	—	—	5.61	15.05	14.65	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JC}$, and T_C. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_C) / R_{\theta JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with MIL-STD-883.

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6.7 Electrical Characteristics for TL06xC and TL06xxC

$V_{CC±}$ = ±15 V, R_L = 10 kΩ to (V_{CC+} + V_{CC-}) / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		TL061C, TL062C, TL064C			TL061AC, TL062AC, TL064AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	15		3	6	mV
			T_A = Full range			20			7.5	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = Full range			10			10		µV/°C
I_{IO} (3)	Input offset current	V_O = 0	T_A = 25°C		5	200		5	100	pA
			T_A = Full range			5			3	nA
I_{IB} (3)	Input bias current(2)	V_O = 0	T_A = 25°C		30	400		30	200	pA
			T_A = Full range			10			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ, T_A = 25°C		±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ, T_A = Full range		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	3	6		4	6		V/mV
			T_A = Full range	3			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ, T_A = 25°C			1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω, T_A = 25°C		70	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC±}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		70	95		80	95		dB
P_D	Total power dissipation (each amplifier)	V_O = 0, No load, T_A = 25°C			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	V_O = 0, No load, T_A = 25°C			200	250		200	250	µA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06xC, TL06xAC, and TL06xBC and –40°C to 85°C for TL06xI.
(2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-12. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
(3) Specified by design and characterization; not production tested.

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6.8 Electrical Characteristics for TL06xxC and TL06xI

$V_{CC±}$ = ±15 V, R_L = 10 kΩ to (V_{CC+} + $V_{CC–}$) / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		TL061BC, TL062BC, TL064BC			TL061I, TL062I, TL064I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		2	3		3	6	mV
			T_A = Full range			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = Full range			10			10		µV/°C
I_{IO} (3)	Input offset current	V_O = 0	T_A = 25°C		5	100		5	100	pA
			T_A = Full range			3			10	nA
I_{IB} (3)	Input bias current(2)	V_O = 0	T_A = 25°C		30	200		30	200	pA
			T_A = Full range			7			20	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ, T_A = 25°C		±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ, T_A = Full range		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	4	6		4	6		V/mV
			T_A = Full range	4			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ, T_A = 25°C			1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC±}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	V_O = 0, No load, T_A = 25°C			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	V_O = 0, No load, T_A = 25°C			200	250		200	250	µA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06xC, TL06xAC, and TL06xBC and –40°C to 85°C for TL06xI.

(2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-12. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

(3) Assured by design and characterization; not production tested.

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6.9 Electrical Characteristics for TL06xM

$V_{CC±}$ = ±15 V, R_L = 10 kΩ to (V_{CC+} + $V_{CC–}$) / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS[2]		TL061M, TL062M			TL064M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	6		3	9	mV
			T_A = –55°C to 125°C			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = –55°C to 125°C			10			10		µV/°C
I_{IO} [4]	Input offset current	V_O = 0	T_A = 25°C		5	100		5	100	pA
			T_A = –55°C			20[1]			20[1]	nA
			T_A = 125°C			20			20	
I_{IB} [4]	Input bias current[3]	V_O = 0	T_A = 25°C		30	200		30	200	pA
			T_A = –55°C			50[1]			50[1]	nA
			T_A = 125°C			50			50	
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ, T_A = 25°C		±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ, T_A = –55°C to 125°C		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	4	6		4	6		V/mV
			T_A = –55°C to 125°C	4			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ, T_A = 25°C			1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC±}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	V_O = 0, No load, T_A = 25°C			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	V_O = 0, No load, T_A = 25°C			200	250		200	250	µA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

(1) This parameter is not production tested.
(2) All characteristics are measured under open-loop conditions, with zero common-mode voltage, unless otherwise specified.
(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-12. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
(4) Specified by design and characterization; not production tested.

6.10 Operating Characteristics

$V_{CC±}$ = ±15 V, T_A= 25°C, R_L = 10 kΩ to (V_{CC+} + $V_{CC–}$) / 2

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain[1]	V_I = 10 V, R_L = 10 kΩ,	C_L = 100 pF, see Figure 7-1	1.5	3.5		V/µs
t_r	Rise-time	V_I = 20 V, R_L = 10 kΩ,	C_L = 100 pF, see Figure 7-1		0.2		µs
	Overshoot factor				10%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		30		nV/√Hz

(1) Slew rate at –55°C to 125°C is 0.7 V/µs min.

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Typical Characteristics

Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.

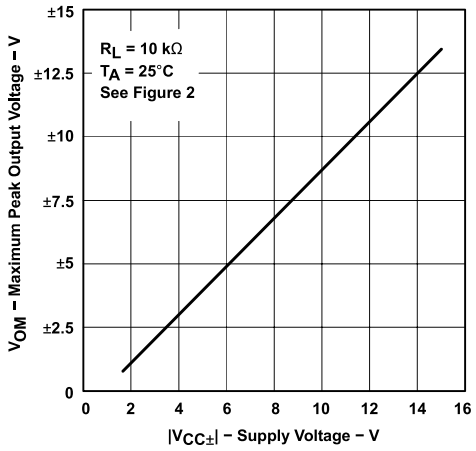

Figure 6-1. Maximum Peak Output Voltage vs Supply Voltage

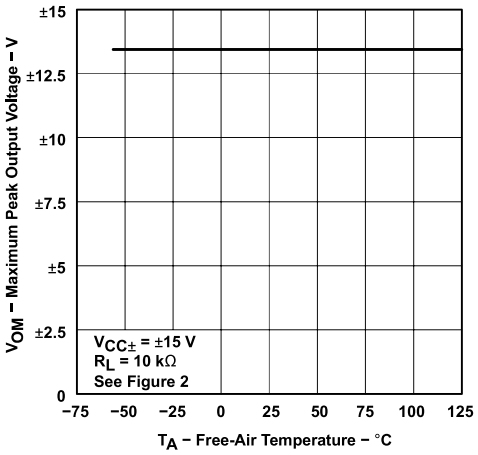

Figure 6-2. Maximum Peak Output Voltage vs Free-Air Temperature

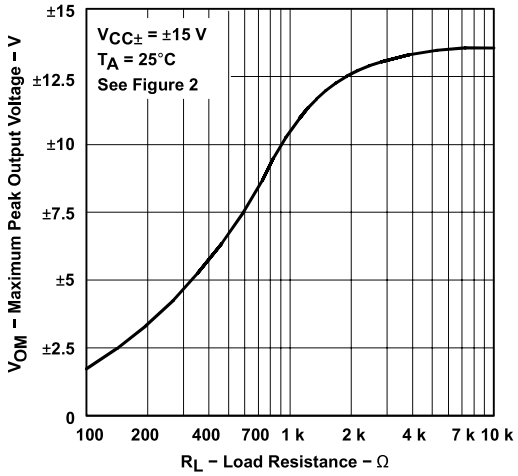

Figure 6-3. Maximum Peak Output Voltage vs Load Resistance

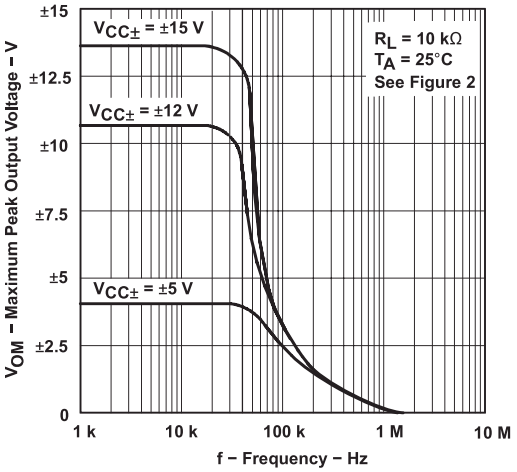

Figure 6-4. Maximum Peak Output Voltage vs Frequency

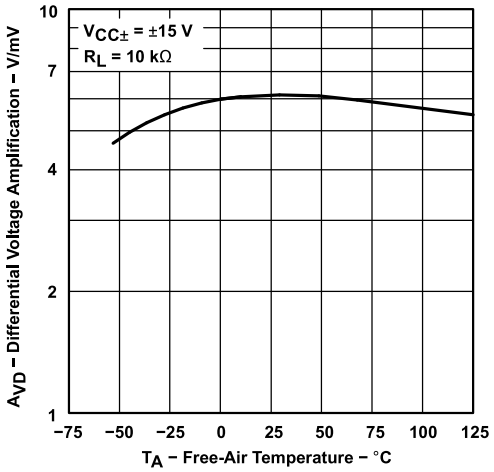

Figure 6-5. Differential Voltage Amplification vs Free-Air Temperature

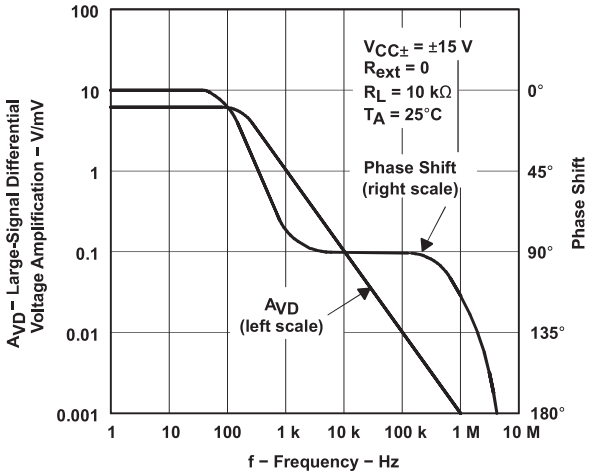

Figure 6-6. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.

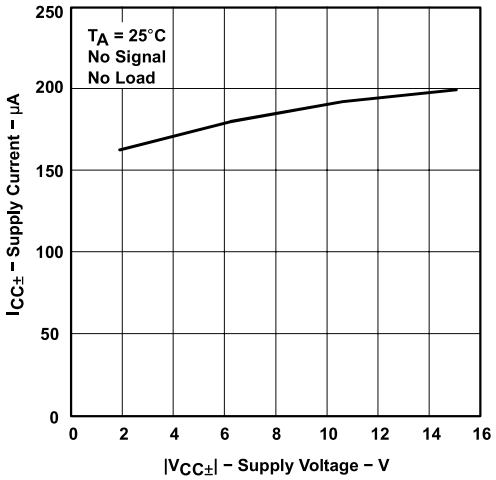

Figure 6-7. Supply Current vs Supply Voltage

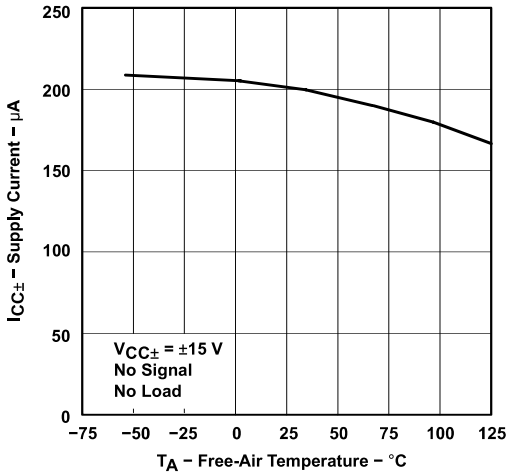

Figure 6-8. Supply Current vs Free-Air Temperature

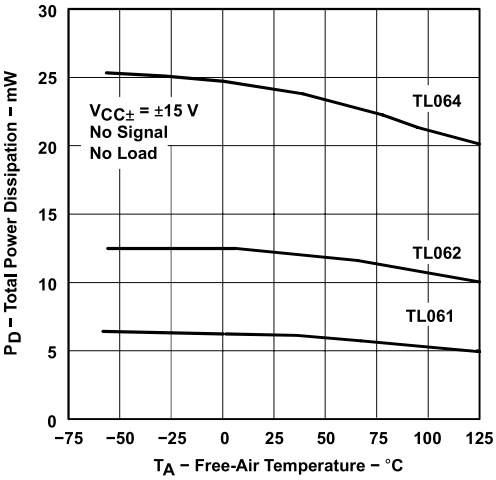

Figure 6-9. Total Power Dissipation vs Free-Air Temperature

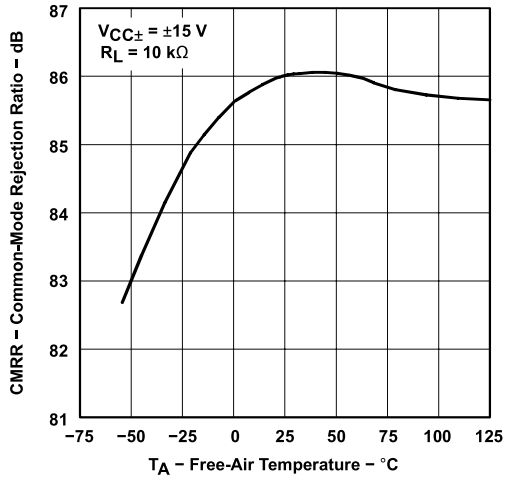

Figure 6-10. All Except TL06_C Common-Mode Rejection Ratio vs Free-Air Temperature

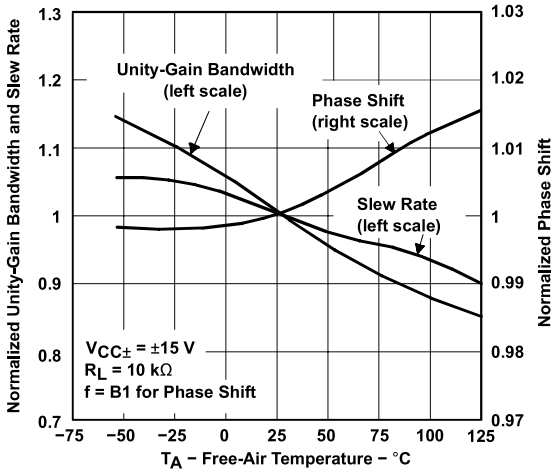

Figure 6-11. Normalized Unity-Gain Bandwidth, Slew Rate, and Phase Shift vs Free-Air Temperature

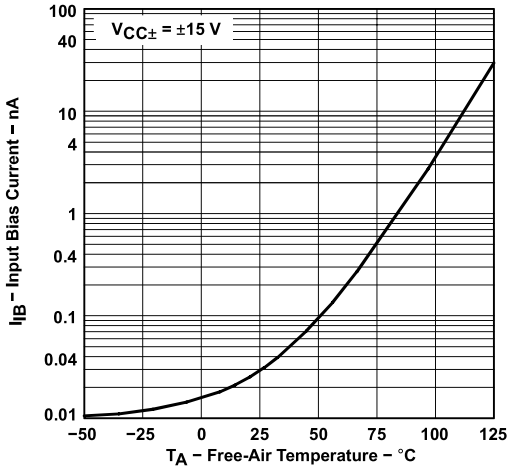

Figure 6-12. Input Bias Current vs Free-Air Temperature

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Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.

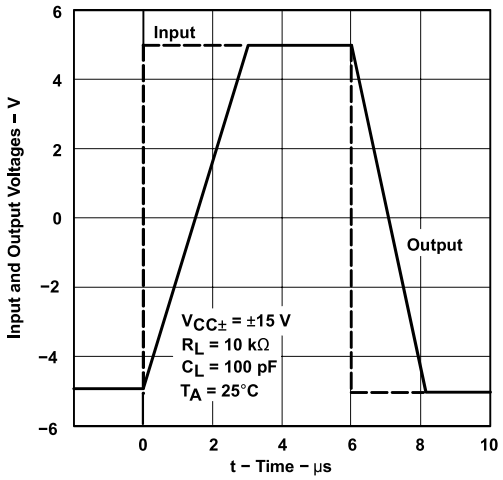

Figure 6-13. Voltage-Follower Large-Signal Pulse Response vs Time

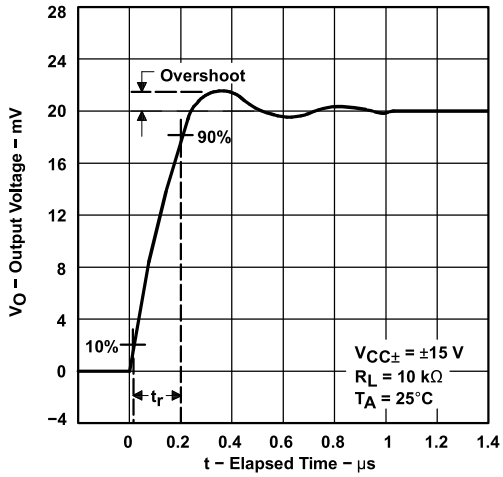

Figure 6-14. Output Voltage vs Elapsed Time

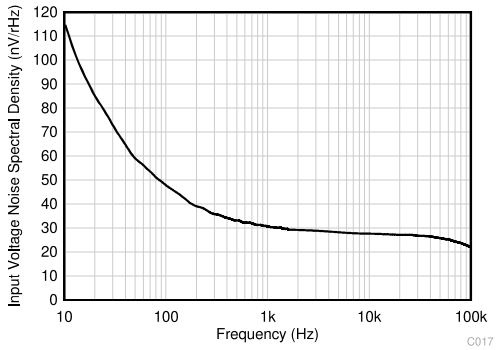

Figure 6-15. Equivalent Input Noise Voltage vs Frequency

7 Parameter Measurement Information

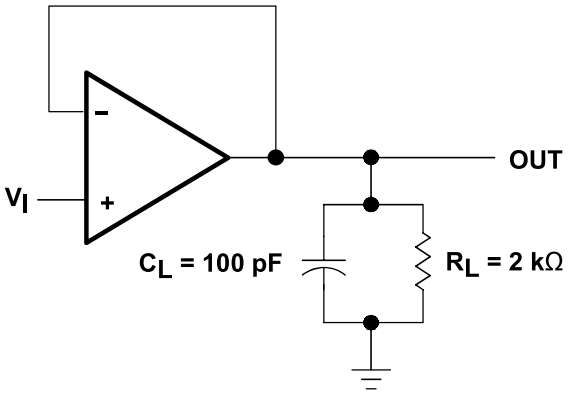

Figure 7-1. Unity-Gain Amplifier

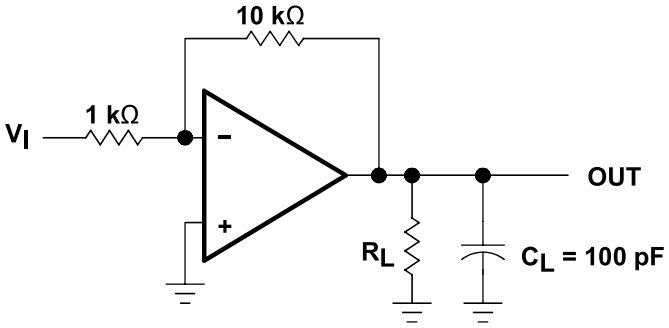

Figure 7-2. Gain-of-10 Inverting Amplifier

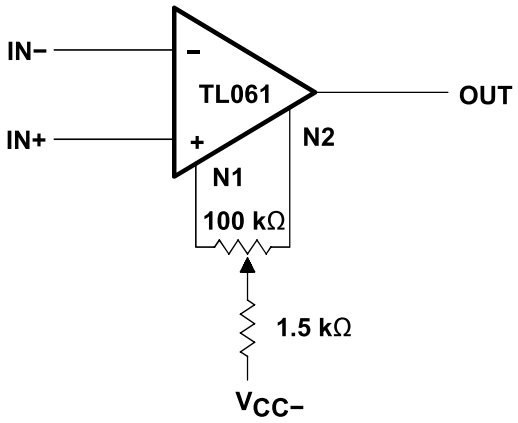

Figure 7-3. Input Offset-Voltage Null Circuit

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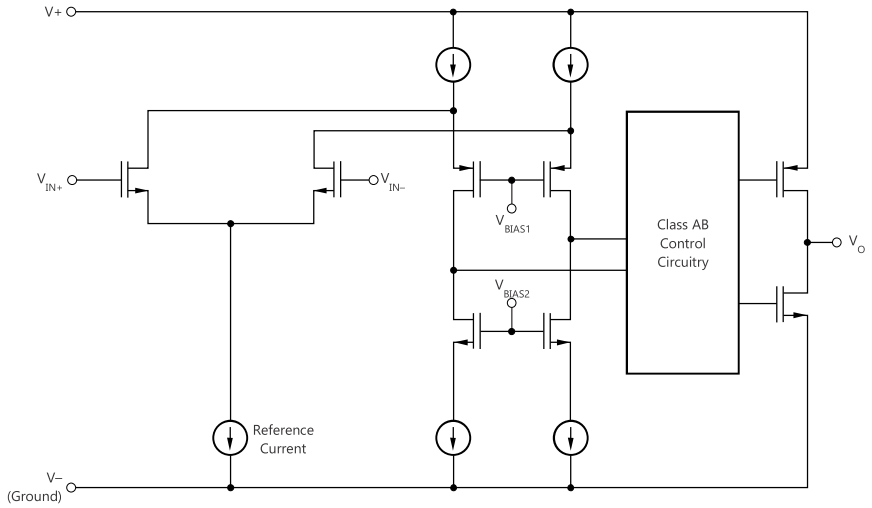
8 Detailed Description

8.1 Overview

The TL06x (TL061, TL062, and TL064) family of industry-standard operational amplifiers (op amps) mirror the TL07x and TL08x family of op amps with lower power consumption. These devices provide outstanding value for cost-sensitive applications, featuring high input impedance, wide bandwidth, high slew rate, and low input offset and input bias currents. High ESD (1.5 kV, HBM), integrated EMI and RF filters, and wide temperature operation enable the TL06x devices to be used in rugged and environmentally-demanding applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C, and the M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. It is found by taking the ratio of the change in input offset voltage to the change in the input voltage and converting to decibels. Ideally the CMRR is infinite, but in practice, amplifiers are designed to have it as high as possible. The CMRR of this device is 86 dB.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 3.5-V/µs slew rate.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

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9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TL06x series of operational amplifiers can be used in countless applications. The few applications in this section show principles used in all applications of these parts.

9.2 Typical Applications

9.2.1 Inverting Amplifier Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

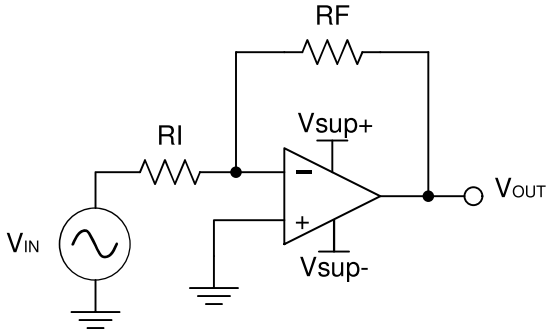

Figure 9-1. Schematic for Inverting Amplifier Application

9.2.1.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

9.2.1.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_V = \frac{VOUT}{VIN} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for RI or RF. Choose a value in the kΩ range to limit currents in the amplifier circuit to the mA range. This example will choose 10 kΩ for RI which means 36 kΩ will be used for RF. This was determined by Equation 3.

$$A_V = -\frac{RF}{RI} \quad (3)$$

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9.2.1.3 Application Curve

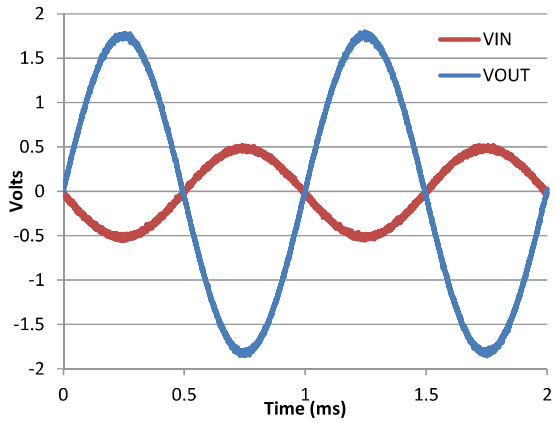

Figure 9-2. Input and Output Voltages of the Inverting Amplifier

9.3 System Examples

9.3.1 General Applications

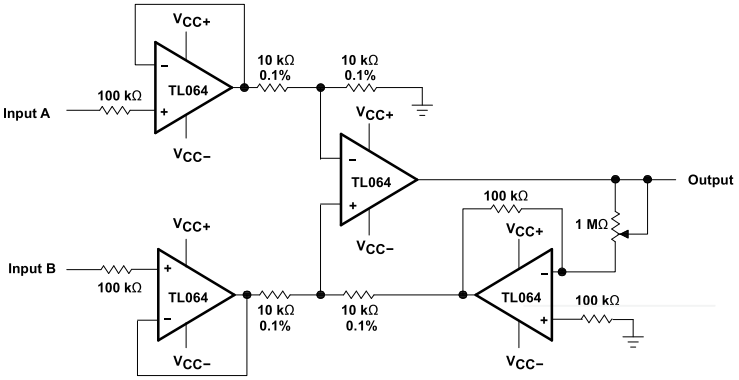

Figure 9-3. Instrumentation Amplifier

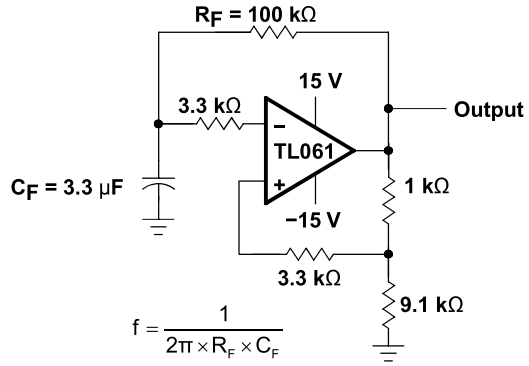

Figure 9-4. 0.5-Hz Square-Wave Oscillator

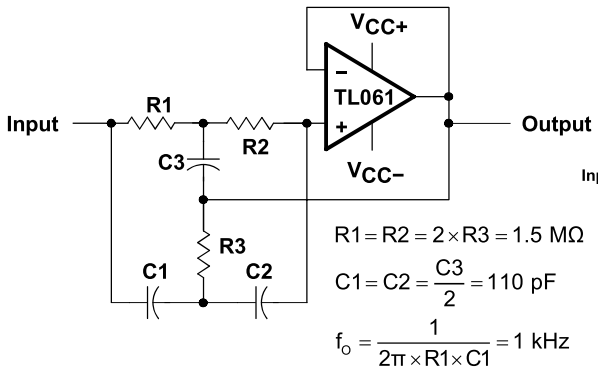

Figure 9-5. High-Q Notch Filter

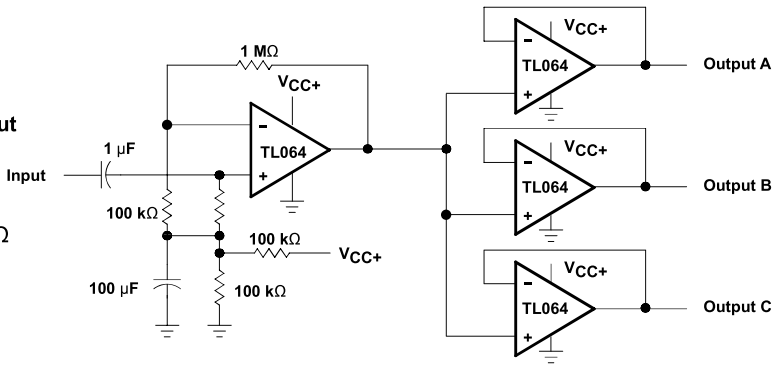

Figure 9-6. Audio-Distribution Amplifier

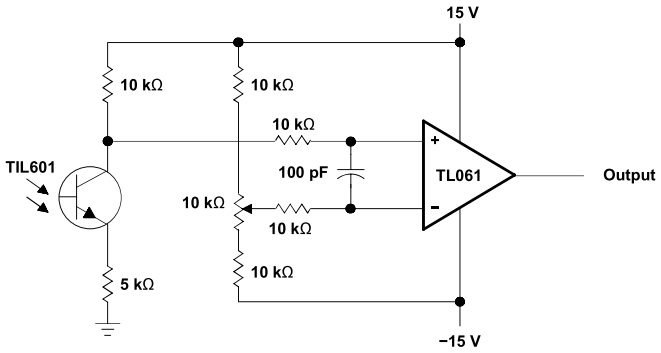

Figure 9-7. Low-Level Light Detector Preamplifier

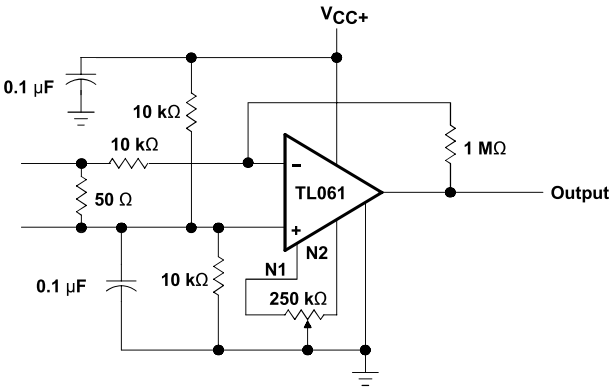

Figure 9-8. AC Amplifier

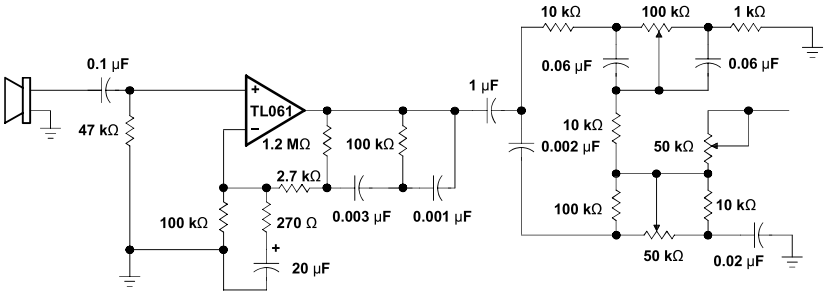

Figure 9-9. Microphone Preamplifier With Tone Control

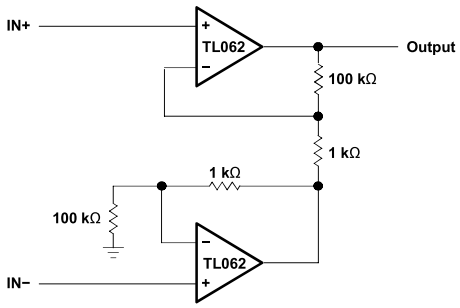

Figure 9-10. Instrumentation Amplifier

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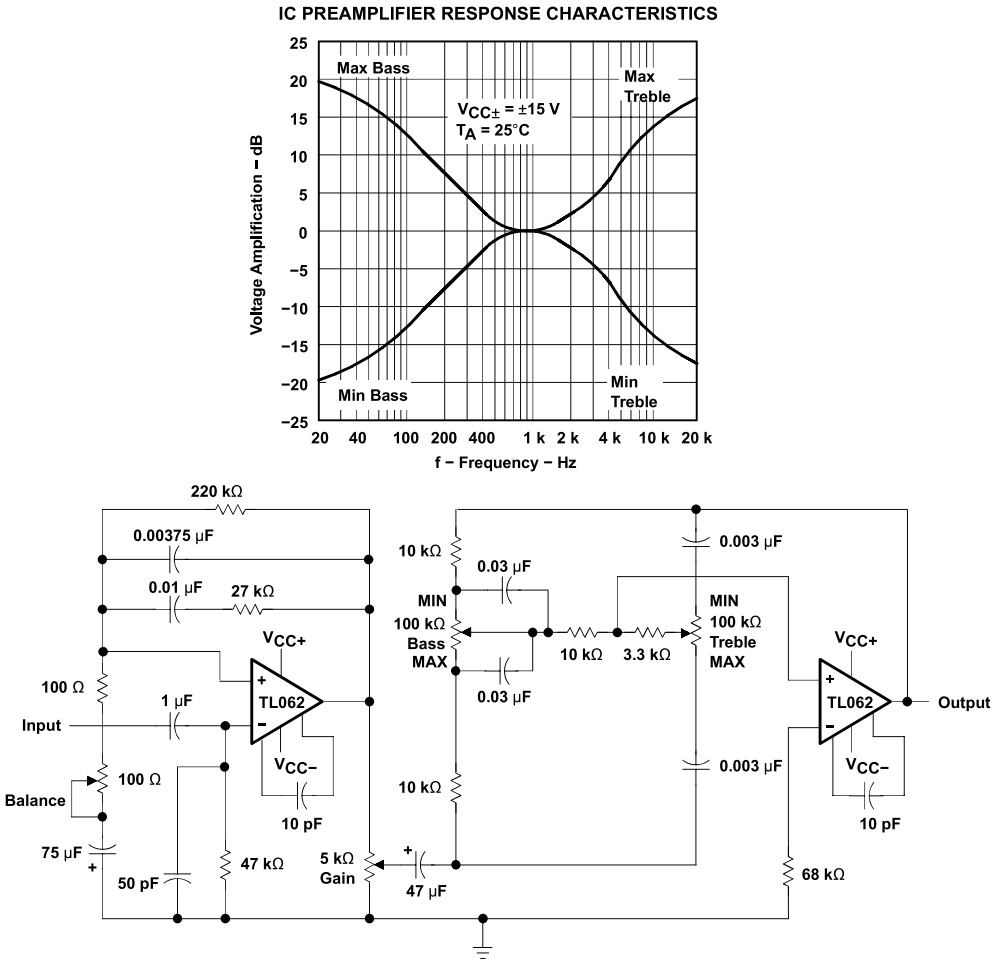

Figure 9-11. IC Preamplifier

9.4 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single supply, or outside the range of ±18 V for a dual supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

9.5 Layout

9.5.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Examples*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

9.5.2 Layout Examples

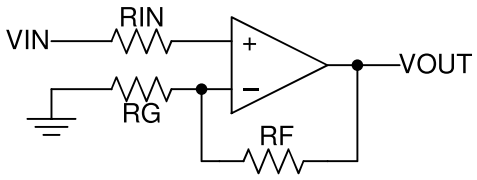

Figure 9-12. Operational Amplifier Schematic for Noninverting Configuration

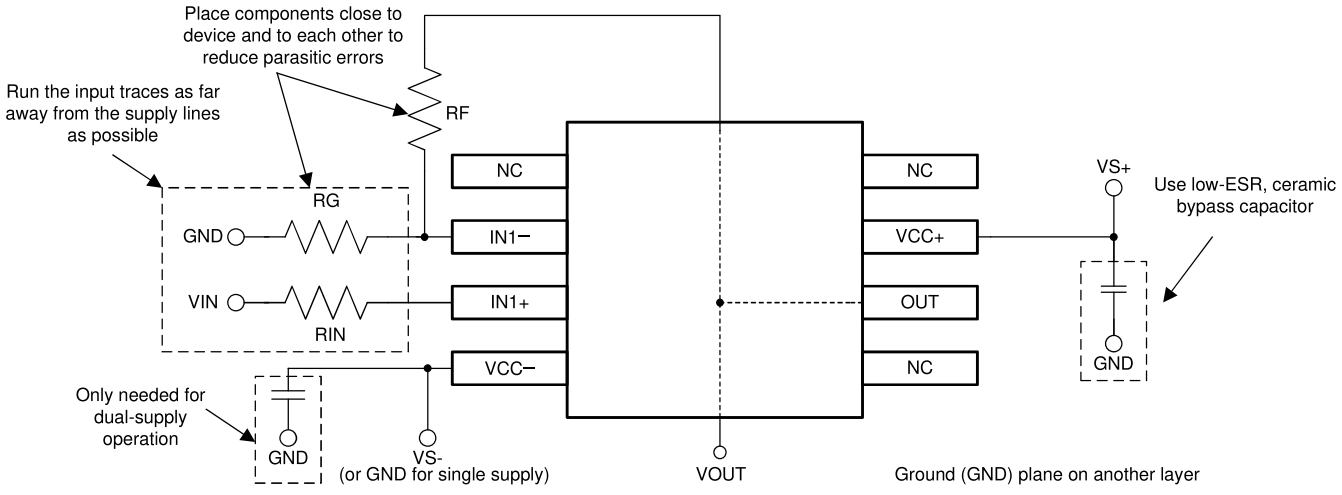

Figure 9-13. Operational Amplifier Board Layout for Noninverting Configuration

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Circuit Board Layout Techniques* chapter extracts

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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